FIG. 1

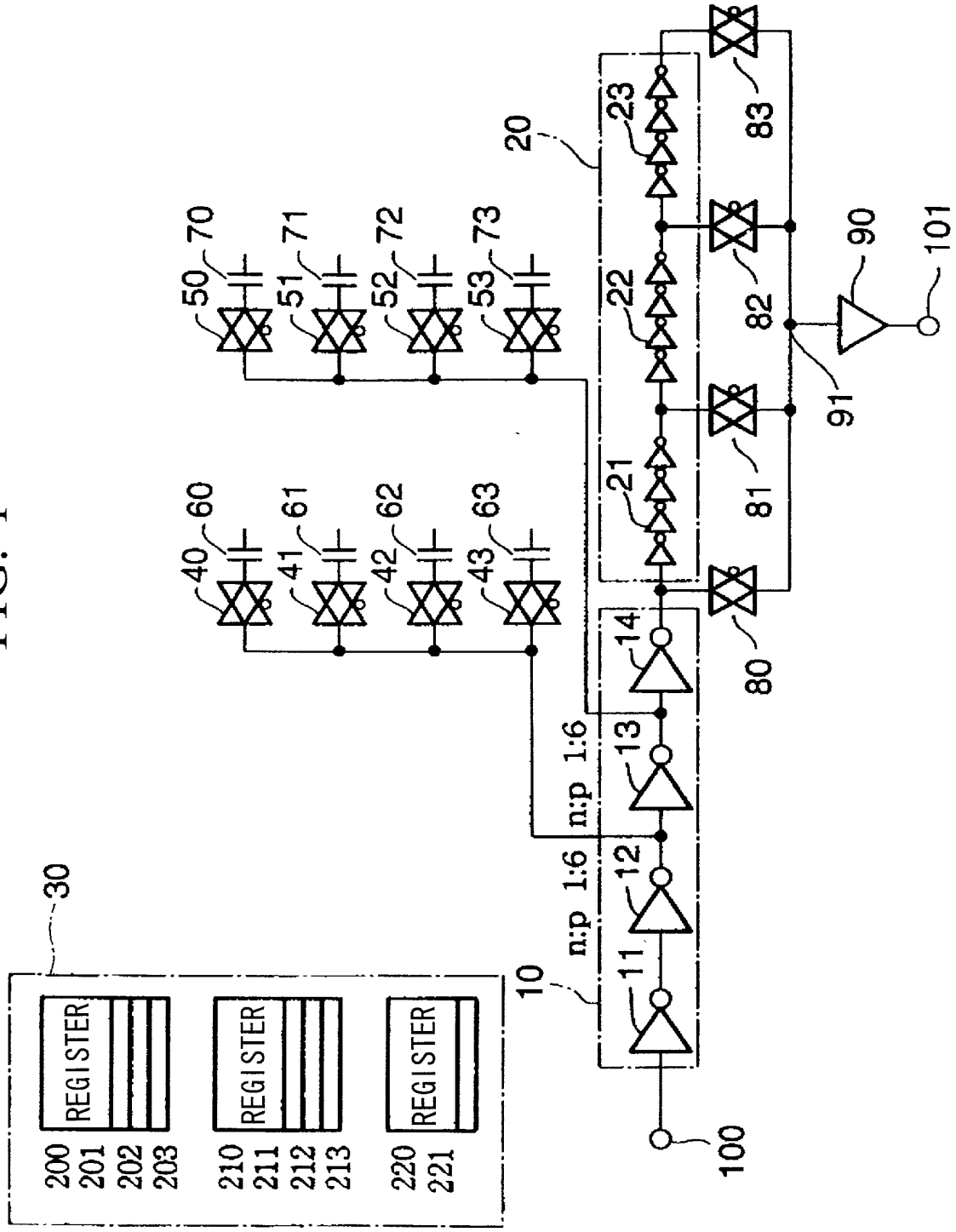

REGISTER
REGISTER
REGISTER
200
201
202
203
210
211
212
213
220
221
30
10
20
n:p 1:6
n:p 1:6
11
12
13
14
21
22
23
40
41
42
43
50
51
52
53
60
61
62
63
70
71
72
73
80
81
82
83
90
91
100
101

FIG. 2

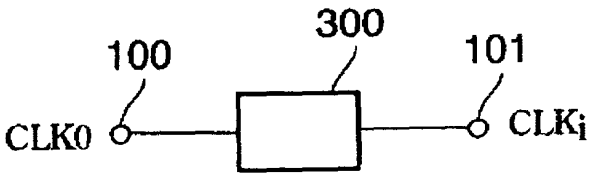


FIG. 4

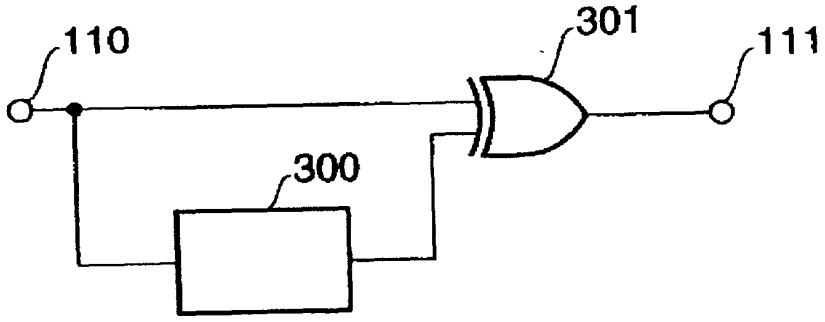


FIG. 8

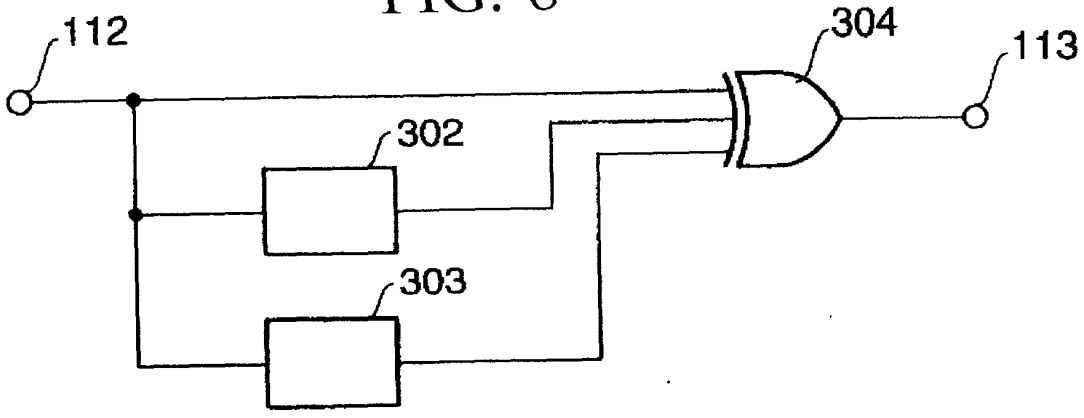


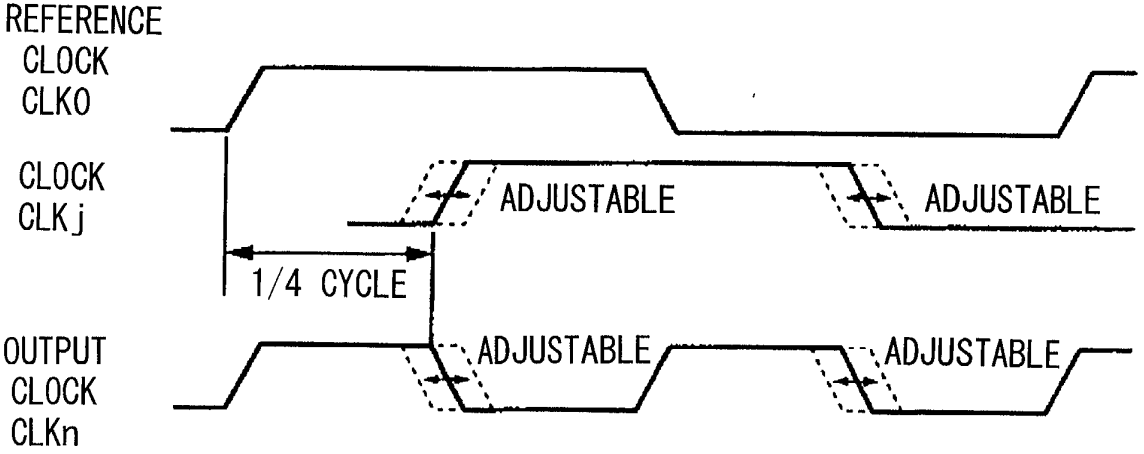
FIG. 3A

FIG. 3B

FIG. 5A

FIG. 5B

FIG. 5C



Title: DELAY ADJUSTMENT CIRCUIT AND A CLOCK GENERATING CIRCUIT USING THE SAME
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FIG. 6A

FIG. 6B

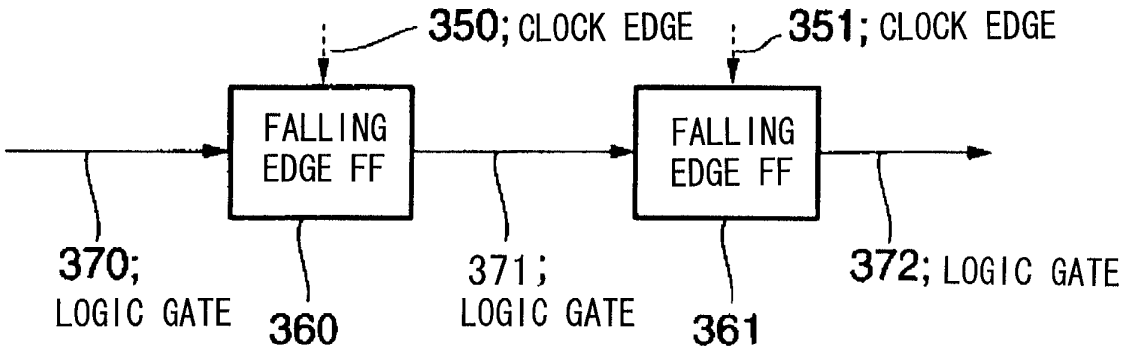

FIG. 9A REFERENCE CLOCK CLK0

FIG. 9B CLOCK CLKx

FIG. 9C CLOCK CLKy

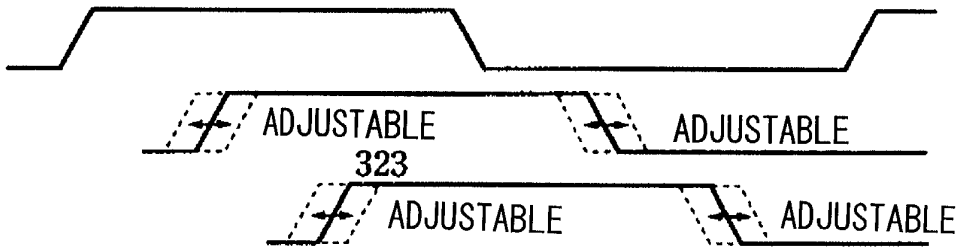

FIG. 9D CLOCK CLKz

Title: DELAY ADJUSTMENT CIRCUIT AND A CLOCK GENERATING CIRCUIT USING THE SAME
Inventor(s): Atsushi YOSHIKAWA, et al
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FIG. 7

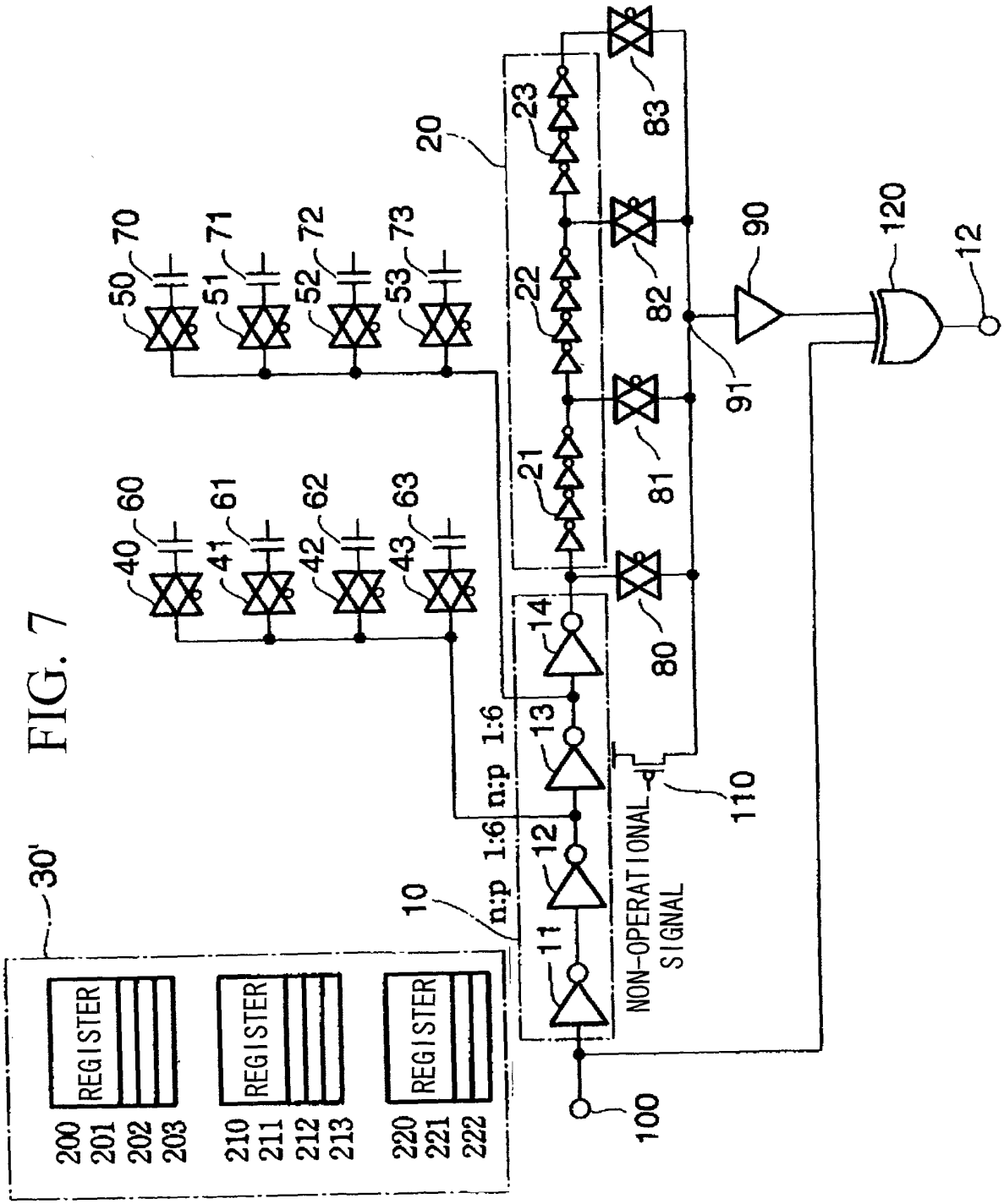

30'
10
20
REGISTER
200
201
202
203
210
211
212
213
220
221
222
n:p 1:6
n:p 1:6
11
12
13
14
NON-OPERATIONAL SIGNAL
110
100
40
41
42
43
60
61
62
63
50
51
52
53
70
71
72
73
80
81
82
83
21
22
23
90
91
120
12

FIG. 10

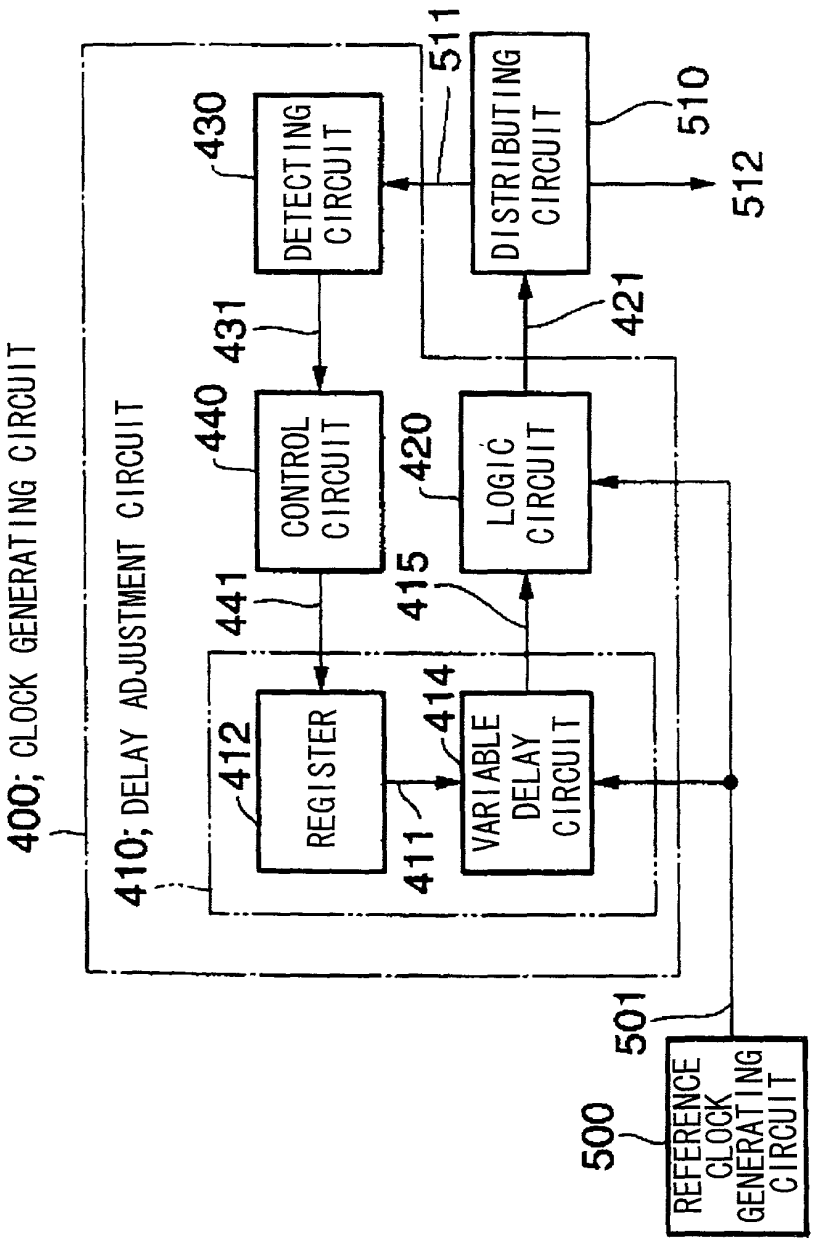

400; CLOCK GENERATING CIRCUIT
410; DELAY ADJUSTMENT CIRCUIT
REGISTER
412
VARIABLE DELAY CIRCUIT
414
411
CONTROL CIRCUIT
440
441
LOGIC CIRCUIT
420
415
DETECTING CIRCUIT
430
431
DISTRIBUTING CIRCUIT
510
511
512
421
REFERENCE CLOCK GENERATING CIRCUIT
500
501

FIG. 11

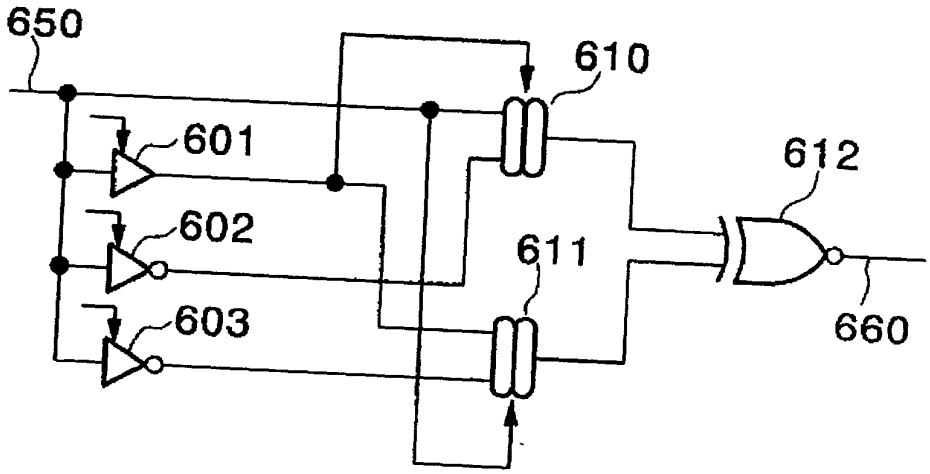

650
610
601
612
602
611
603
660

FIG. 13

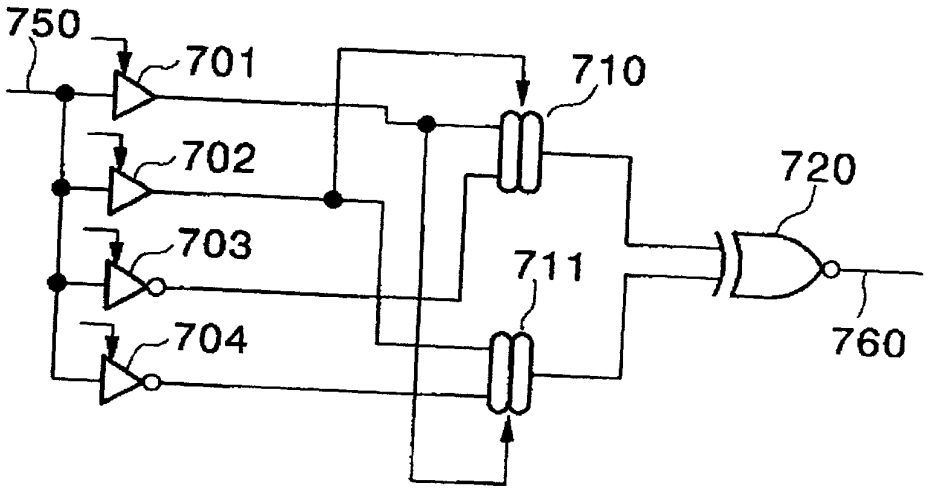

750
701
710
702
720
703
711
704
760

FIG. 12A INPUT SIGNAL 650

FIG. 12B OUTPUT SIGNAL OF 601

FIG. 12C 2/4 CYCLE DELAYED SIGNAL OF 650

FIG. 12D OUTPUT SIGNAL OF 602 3/4 CYCLE DELAYED

FIG. 12E SIGNAL OF INPUT SIGNAL 650

FIG. 12F OUTPUT SIGNAL OF 603

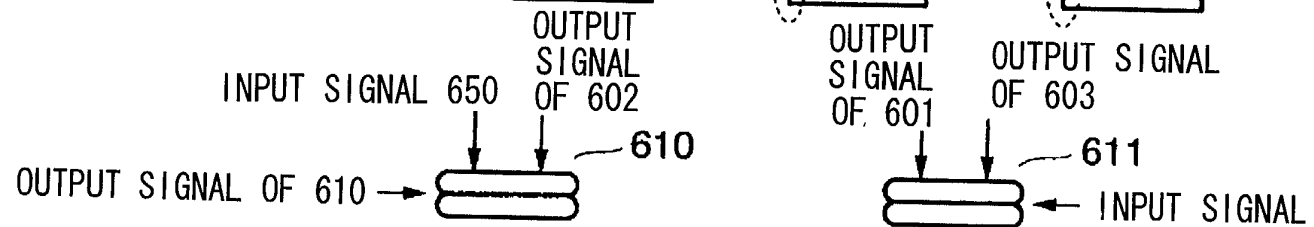
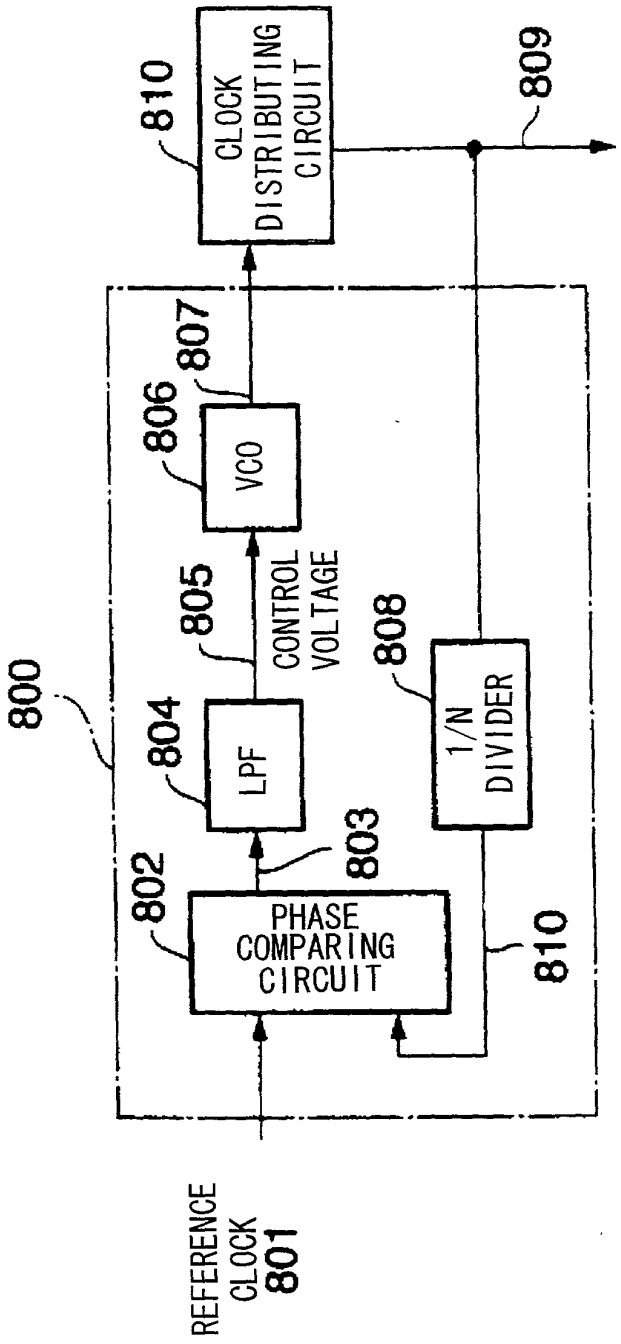


FIG. 12G OUTPUT SIGNAL OF 601

FIG. 12H OUTPUT SIGNAL OF 611

FIG. 12I OUTPUT SIGNAL 660

FIG. 14


800
REFERENCE CLOCK
801
PHASE COMPARING CIRCUIT
802
803
LPF
804
CONTROL VOLTAGE
805
VCO
806
807
1/N DIVIDER
808
CLOCK DISTRIBUTING CIRCUIT
809
810
810